Kodak
Image Sensor Solutions

PRELIMINARY DEVICE PERFORMANCE SPECIFICATION

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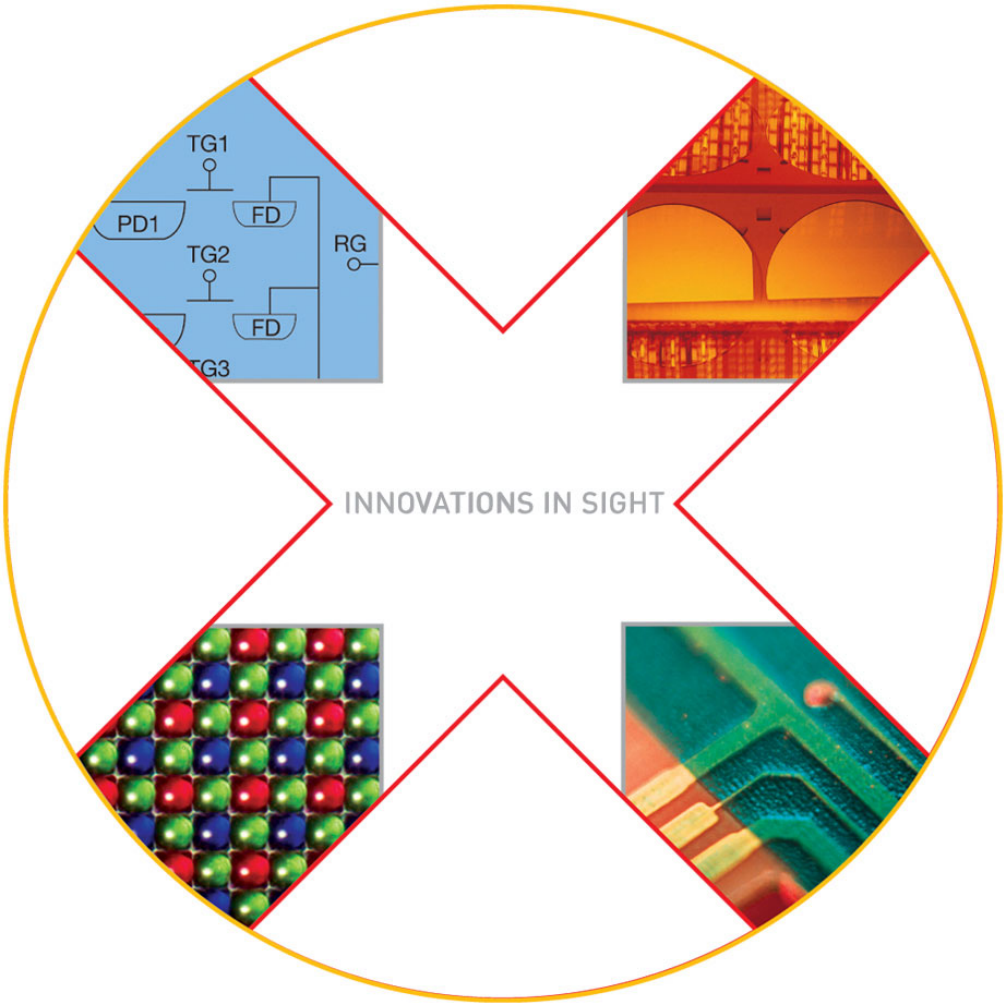


KODAK KAF-16803 IMAGE SENSOR

4096 (H) X 4096 (V) FULL-FRAME CCD IMAGE SENSOR

** THE OUTPUT GATE BIAS WAS CHANGED BEFORE THIS PART WAS RELEASED TO PRODUCTION. EARLY SAMPLES, SN100 THROUGH 150, USE V_{OG} = 6.0 , WHILE LATER PARTS, BEGINNING WITH SN=151, USE V_{OG} = 2.0 (SEE PAGE 18).

Kodak
Image Sensor Solutions

TABLE OF CONTENTS

TABLE OF FIGURES

Kodak
Image Sensor Solutions

SUMMARY SPECIFICATION

KODAK KAF-16803 IMAGE SENSOR

4096 (H) X 4096 (V) FULL FRAME CCD IMAGE SENSOR

DESCRIPTION

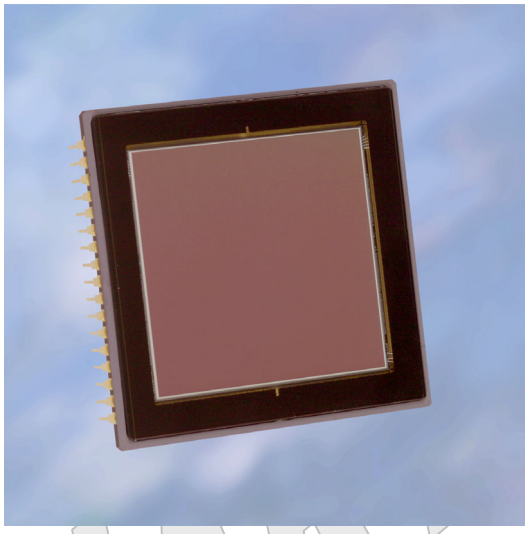
The KAF-16803 image sensor is a redesigned version of the popular KAF-16801E image sensor (4096 x 4096 pixel resolution) with enhancements that specifically target the needs of high performance digital radiography applications. Improvements include enhanced quantum efficiency for improved DQE at higher spatial frequencies, lower noise for improved contrast in areas of high density, and anti-blooming protection to prevent image bleed from over exposure in regions outside the patient. Utilizing Kodak's proprietary single gate ITO process and micro-lens technology, the KAF-16803 image sensor with its large imaging area and small pixel size provides the sensitivity, resolution and contrast necessary for high quality digital radiographs. To simplify device integration, the KAF-16803 image sensor uses the same pin-out and package as the KAF-16801E image sensor.

FEATURES

- High Resolution
- Large Image Area
- High Quantum Efficiency
- Low Noise Architecture
- Broad Dynamic Range

APPLICATIONS

- Digital radiography
- Astronomy
- Life Sciences



Parameter	Typical Value
Architecture	Full Frame CCD; with Square Pixels
Total Number of Pixels	4145 (H) x 4128 (V) = 17.1 Mp
Number of Effective Pixels	4127 (H) x 4128 (V) = 17 Mp
Number of Active Pixels	4096(H) x 4096 (V) = 16.8 Mp
Pixel Size	9 µm (H) x 9 µm (V)
Chip Size	38.6 mm (H) x 37.76mm (V)
Aspect Ratio	square
Saturation Signal	85 K e^-
Charge to Voltage Conversion	22 µV/e^-
Quantum Efficiency (550nm))	60%
Responsivity (550 nm)	1302 ke/µJ/cm2 28.7 V/µJ/cm2
Read Noise (f=4 MHz)	9 e^-
Dark Signal (T=25°C)	3 e/pix/sec
Dark Current Doubling Temperature	6.6° C
Linear Dynamic Range (f=4 MHz, T=25 C)	76 dB
Blooming Protection (4ms exposure time)	> 100X saturation exposure
Maximum Data Rate	10 MHz

All parameters above are specified at T = 25 ° C

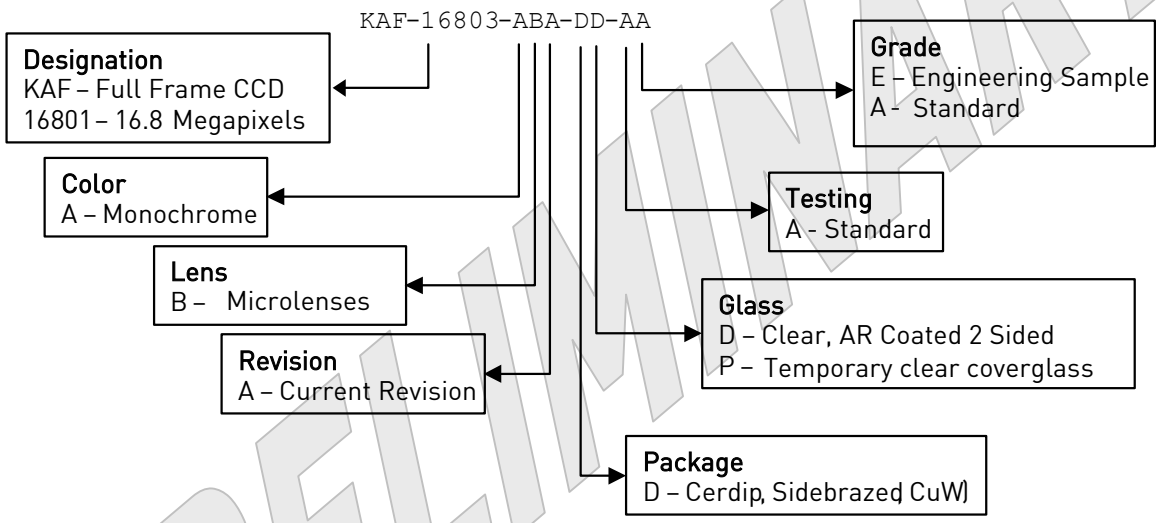
ORDERING INFORMATION

AVAILABLE PART CONFIGURATIONS

The Marking Code on the back of each part is the same for all ordering options, consisting of the text 'KAF-16803-ABA' followed by the serial number of the part.

Available Part Numbers	Description
KAF-16803-ABA-DD-AA	Monochrome, Microlens, CERDIP Package (sidebrazed, CuW), AR coated 2 sides, Standard grade
KAF-16803-ABA-DD-AE	Monochrome, Microlens, CERDIP Package (sidebrazed, CuW), AR coated 2 sides, Engineering sample
KAF-16803-ABA-DP-AA	Monochrome, Microlens, CERDIP Package (sidebrazed, CuW), Temporaryclear coverglass, Standard grade
KAF-16803-ABA-DP-AE	Monochrome, Microlens, CERDIP Package (sidebrazed, CuW), Temporary clear coverglass, Engineering sample

Please contact Image Sensor Solutions for available part numbers.



DEVICE DESCRIPTION

ARCHITECTURE

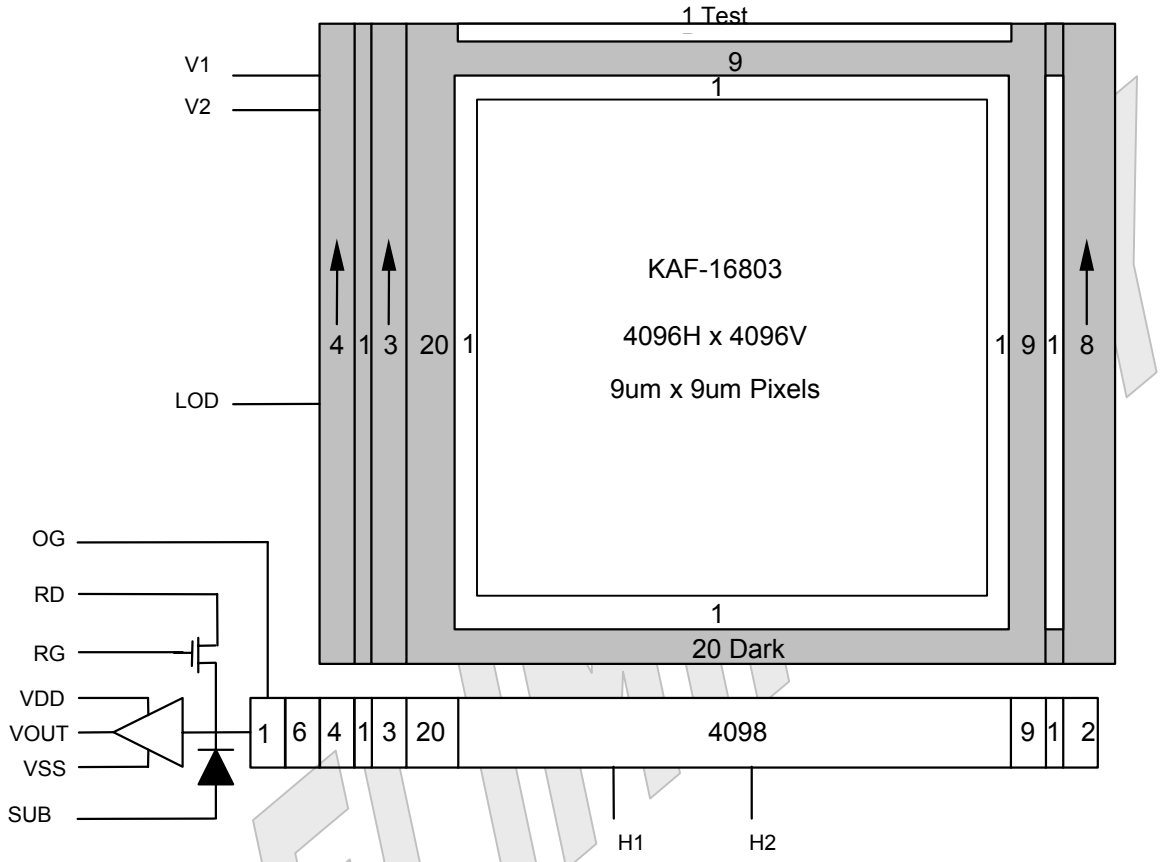


Figure 1 - Block Diagram

DARK REFERENCE PIXELS

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region, exist light shielded pixels that include 20 leading dark pixels on every line. There are also 20 full dark lines at the start and 9 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a *dark reference*.

DUMMY PIXELS

Within each horizontal shift register there are 11 leading pixels. These are designated as *dummy pixels* and should not be used to determine a dark reference level.

INTERNAL TEST

There are some pixels within each line that may not represent dark signal or the signal in the dummy pixels. These are introduced into the design to facilitate production testing. These behave differently than the buffer and dark pixels and should not be used to establish a dark reference.

ACTIVE BUFFER PIXELS

There is 1 photoactive buffer row and column adjacent to the valid photoactive pixels. These may have signals levels different from those in the imaging array and are not counted in the active pixel count.

IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

CHARGE TRANSPORT

The integrated charge from each pixel is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCDs to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented a new line on the falling edge of V2 while H1 is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion.

HORIZONTAL REGISTER

Output Structure

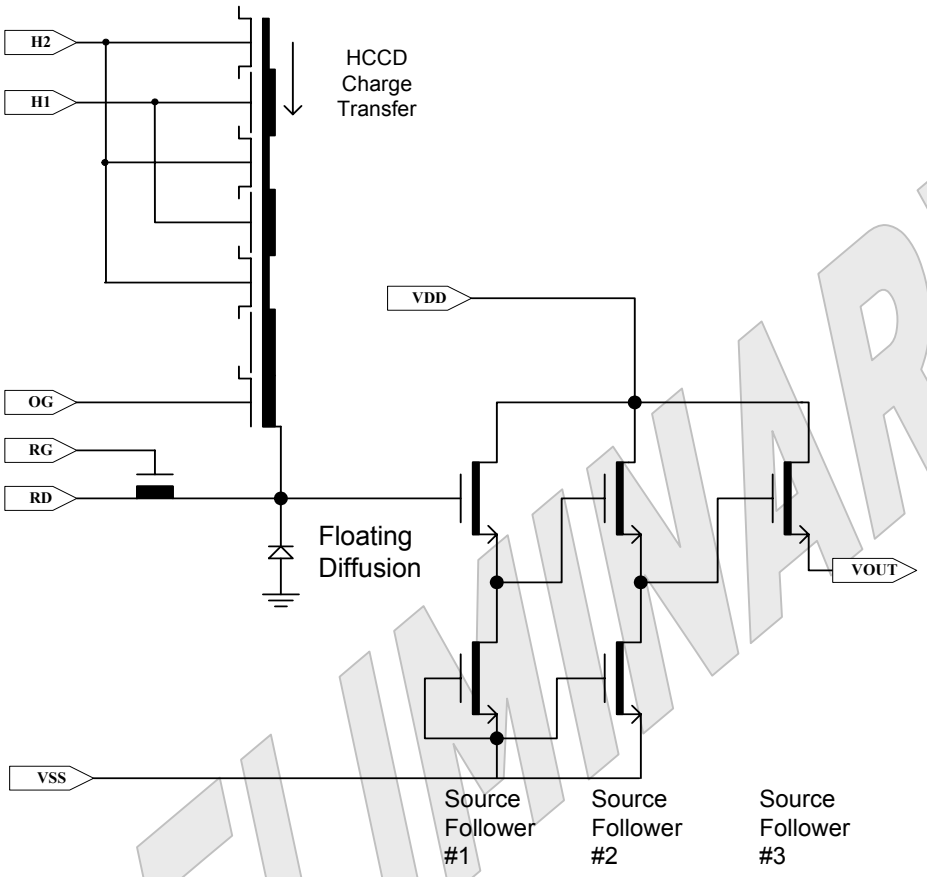


Figure 2 - Output Architecture

The output consists of a floating diffusion capacitance connected to a three-stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip current source must be added to the VOUT pin of the device. See Figure 3.

Output Load

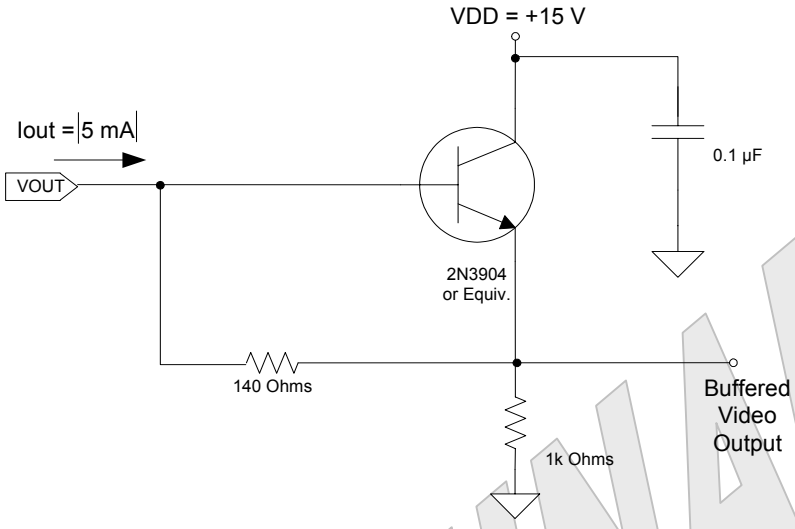
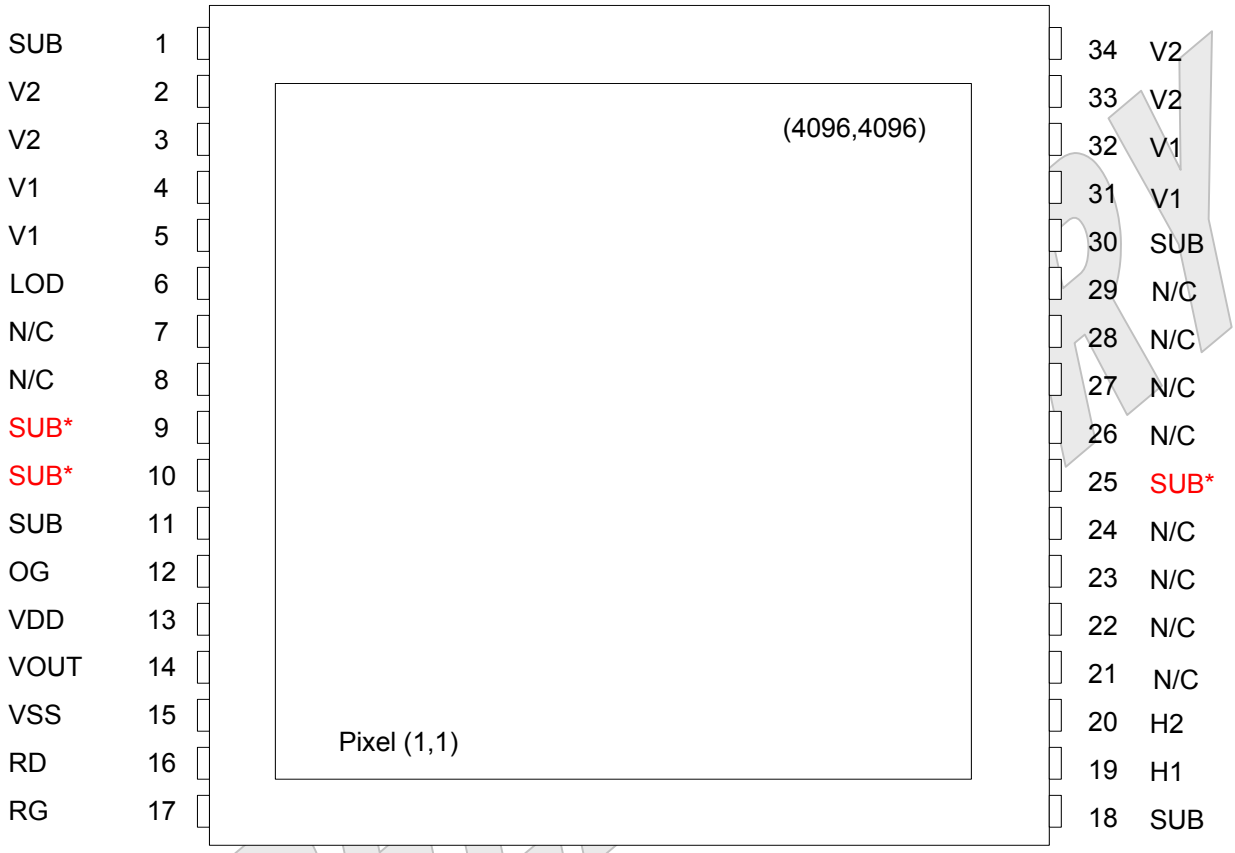


Figure 3 - Recommended Output Structure Load Diagram.
Note: Component values may be revised based on operating conditions and other design considerations.

PHYSICAL DESCRIPTION

PIN DESCRIPTION AND DEVICE ORIENTATION



Note: Pins with the same name are to be tied together on the circuit board and have the same timing.

Notes:

* Unlike the KAF-16801E, pins 9, 10, and, 25 are internally connected to SUB. They may be connected to SUB on the printed circuit board or must be left floating

PIN DESCRIPTION TABLE

Pin	Name	Description
1	SUB	Substrate
2	V2	Vertical CCD Clock-Phase 2
3	V2	Vertical CCD Clock-Phase 2
4	V1	Vertical CCD Clock-Phase 1
5	V1	Vertical CCD Clock-Phase 1
6	LOD	Anti Blooming Drain
7	N/C	No Connection
8	N/C	No Connection
9	SUB*	Substrate or No Connection
10	SUB*	Substrate or No Connection
11	SUB	Substrate
12	OG	Output Gate
13	VDD	Output Amplifier Supply
14	VOUT	Video Output:
15	VSS	Output Amplifier Return
16	RD	Reset Drain
17	RG	Reset Gate
18	SUB	Substrate
19	H1	Horizontal Phase 1
20	H2	Horizontal Phase 2
21	N/C	No Connection
22	N/C	No Connection
23	N/C	No Connection
24	N/C	No Connection
25	SUB*	Substrate or No Connection
26	N/C	No Connection
27	N/C	No Connection
28	N/C	No Connection
29	N/C	No Connection
30	SUB	Substrate
31	V1	Vertical CCD Clock-Phase 1
32	V1	Vertical CCD Clock-Phase 1
33	V2	Vertical CCD Clock-Phase 2
34	V2	Vertical CCD Clock-Phase 2

Notes:

Unlike the KAF-16801E, pins 9, 10, and, 25 are internally connected to SUB. They may be connected to SUB on the printed circuit board or must be left floating

PERFORMANCE

IMAGE PERFORMANCE OPERATIONAL CONDITIONS

Description	Condition - Unless otherwise noted	Notes
Frame time ($t_{readout}$ + t_{int})		Includes overclock pixels
Integration time (tint)	variable	
Horizontal clock frequency	4 MHz	
Temperature	25°C	Room temperature
Mode	integrate – readout cycle	
Operation	Nominal operating voltages and timing with min. vertical pulse width t_{Vw} = 20 µs	

IMAGE PERFORMANCE SPECIFICATIONS

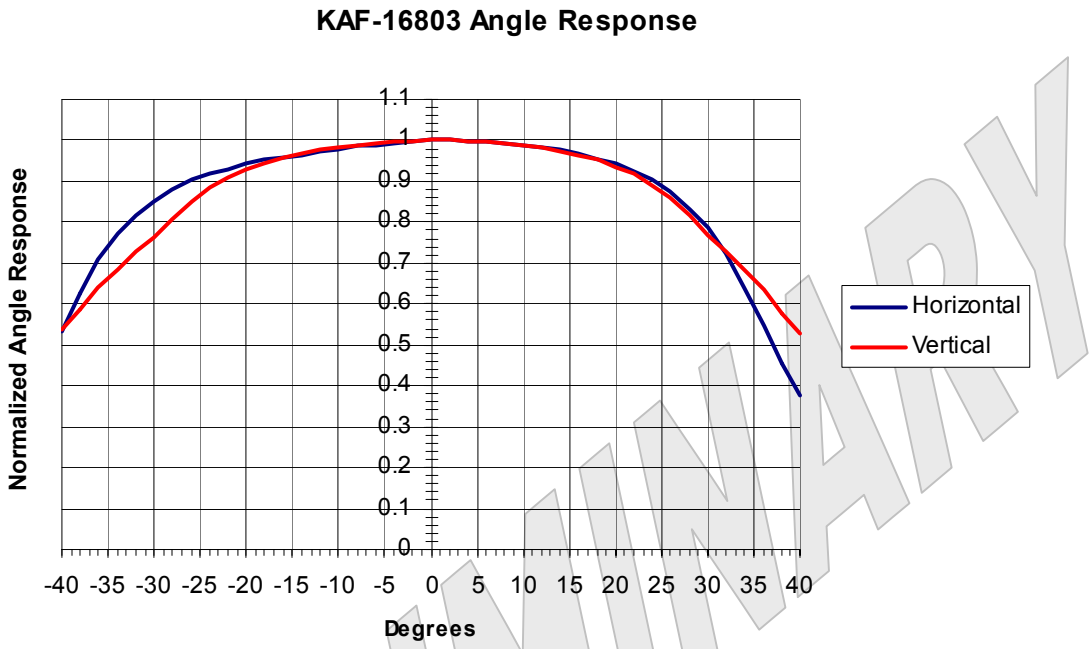
Description	Symbol	Min.	Nom.	Max.	Units	Notes	Sample Plan
Saturation Signal	Ne^-_{sat}		85k		e^-		die
Quantum Efficiency 550 nm	Rg		60		%QE	1	design
Photoresponse Non-Linearity	PRNL		1		%	2	
Photoresponse Non-Uniformity	PRNU		1		%	3	
Integration Dark Signal	Vdark,int		3 0.6	15 3	e/pix/sec pA/cm^2	4	die
Readout Dark Current	Vdark,read		45	225	electrons		
Dark Signal Non-Uniformity	DSNU				e/pix/sec	5	die
Dark Signal Doubling Temperature	ΔT		6.3		°C		design
Read Noise	NR		9		e^- rms	6	die
Linear Dynamic Range	DR		76		dB	7	design
Blooming Protection	X_ab	100			x Esat	8	design
Output Amplifier Sensitivity	Vout/Ne^-		22		µV/e		
DC Offset, output amplifier	Vodc		Vrd – 3.0		V	9	die
Output Amplifier Bandwidth	f_{-3dB}		100		MHz		design
Output Impedance, Amplifier	ROUT		160		Ohms		die

Notes:

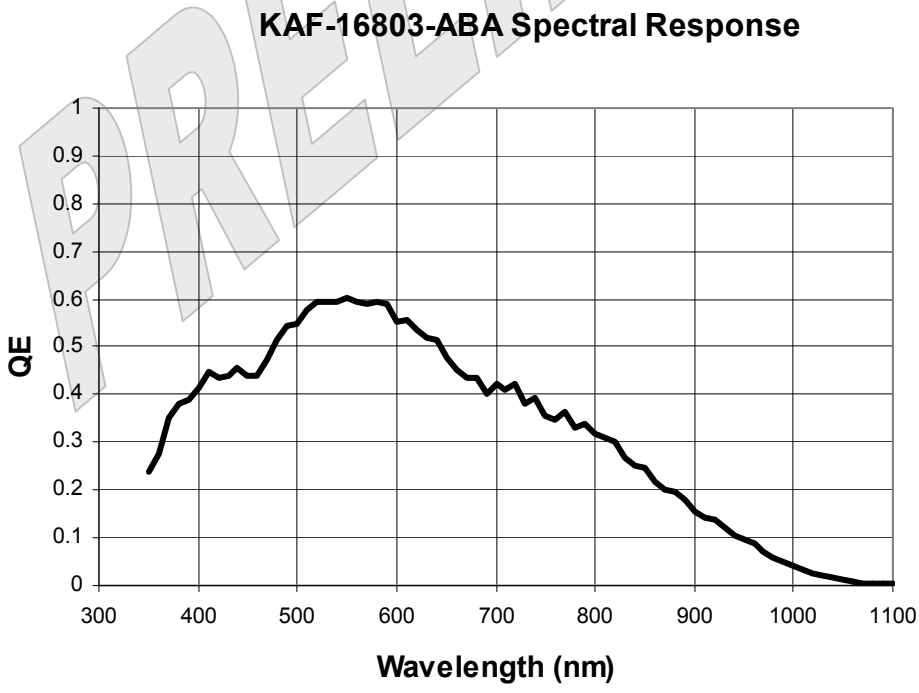
1. Increasing output load currents to improve bandwidth will decrease these values.
2. Worst case deviation from straight line fit, between 1% and 90% of Vsatmin.
3. One Sigma deviation of a 128x128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25 °C.
5. Average dark signal of any of 32 x 32 blocks within the sensor. (each block is 128 x 128 pixels)
6. Output amplifier noise at 25 °C ,operating at pixel frequency up to 4MHz, bandwidth <10MHz , tint = 0, and no dark current shot noise.
7. $20\log(Vsat/V_N)$
8. X_ab is the number of times above the Vsat illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. X_ab is measured at 4ms.
9. Video level offset with respect to ground.

PERFORMANCE CURVES

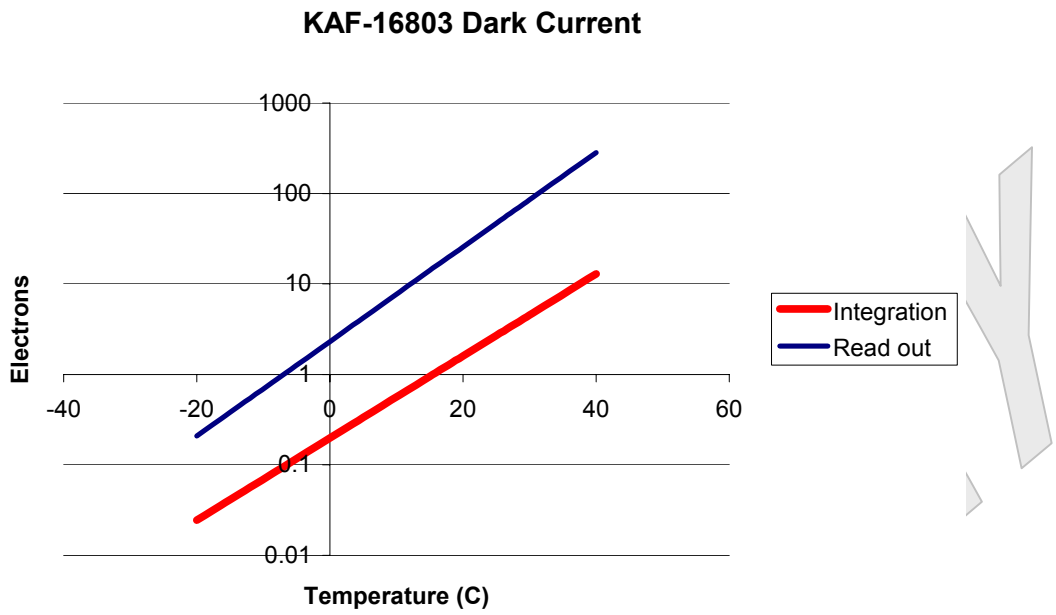
Angle Response



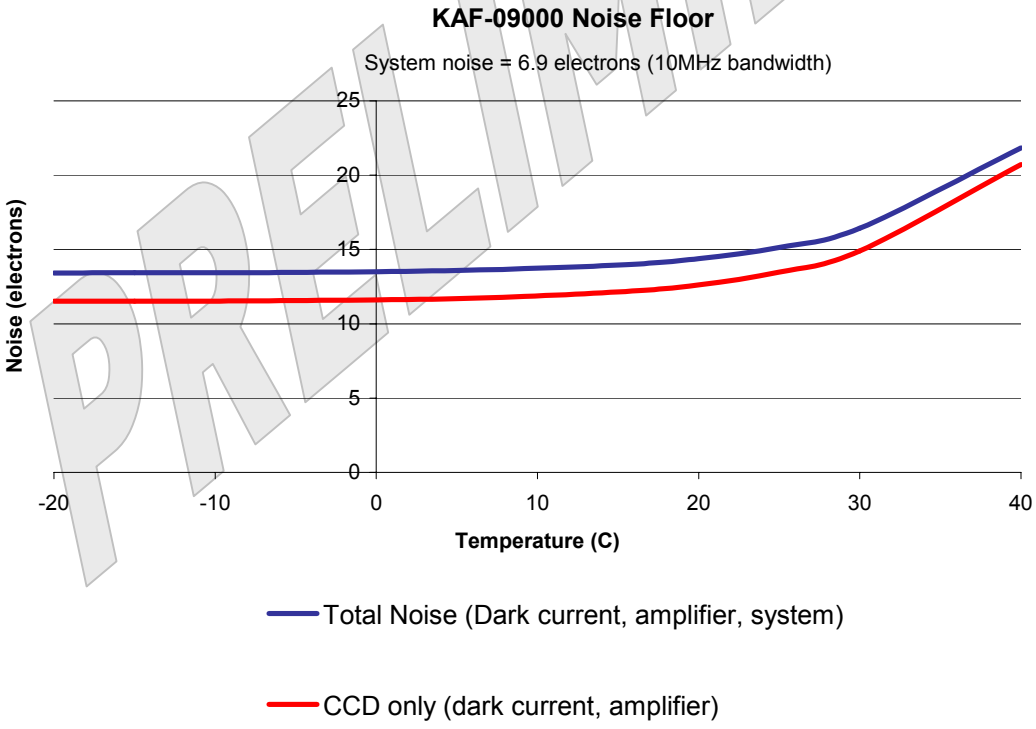
Spectral Response



Dark Signal



Noise Floor



COSMETIC SPECIFICATIONS

Cosmetic Operational Conditions

All cosmetic tests performed at T ~25 °C

Points	Clusters	Columns
<200	<20	<10

Definitions

Point Defects

Dark: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation

-- OR --

Bright: A Pixel with dark current >3,000 e/pixel/sec at 25C

Cluster Defect

A grouping of not more than 10 adjacent point defects

Cluster defects are separated by no less than 4 good pixels in any direction

Column Defect

A grouping of more than 10 point defects along a single column

-- OR --

A column containing a pixel with dark current > 15,000e/pixel/sec (bright column)

-- OR --

A column that does not meet the CTE specification for all exposures less than the specified Max sat. signal level and greater than 2 Ke

-- OR --

A column that contains a pixel which loses more than 250 e under 2Ke illumination (trap defect)

Column defects are separated by no less than 4 good columns. No multiple column defects (double or more) will be permitted.

Column and cluster defects are separated by at least 4 good columns in the x direction.

OPERATION

ABSOLUTE MAXIMUM RATINGS

Description[9]	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{diode}	-0.5	+20	V	1,2
Gate Pin Voltages	V_{gate1}	-16	+16	V	1,3
Adjacent Gate Voltages	V_{1-2}	-16	+16	V	4
Output Bias Current	I_{out}		-30	mA	5
LODT Diode Voltage	V_{LODT}	-0.5	+13.0	V	1
Operating Temperature	T_{OP}	-60	60	°C	7

Notes:

1. Referenced to pin VSUB
2. Includes pins: VRD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H2, RG, VOG.
4. Voltage difference between adjacent gates. Includes: V1 to V2; H1 to H2; H1 to VOG; and V1 to H2.
5. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity).
6. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.
7. Noise performance will degrade at higher temperatures.

POWER-UP SEQUENCE

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (VSUB).
2. Supply the appropriate biases and clocks to the remaining pins.

DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	V_{RD}		13		V	I_{RD} = 0.01	
Output Amplifier Return	VV_{SS}		2.0		V	I_{SS} = 3.0	
Output Amplifier Supply	VV_{DD}		15.0		V	I_{OUT} + I_{SS}	
Substrate	V_{SUB}		0		V	0.01	
Output Gate (SN100 – 150)	V_{OG}		6.0**		V	0.01	
Output Gate (SN151 and greater)	V_{OG}		2.0**		V	0.01	
Lateral Overflow Drain	V_{LOD}		8.0		V	0.01	
Video Output Current	I_{OUT}		-5		mA		1

** The output gate bias was changed before this part was released to production. Early samples, SN100 through 150, use V_{OG} = 6.0 , while later parts, beginning with SN=151, use V_{OG} = 2.0

Notes:

1. An output load sink must be applied to VOUT to activate output amplifier – see Figure 3.

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance	Notes
V1 Low Level	V1L	Low		-9.0		V	250 nF	1
V1 High Level	V1H	High		2.5		V		1
V2 Low Level	V2L	Low		-9.0		V	250 nF	1
V2 High Level	V2H	High		2.5		V		1
H1 Low Level	H1L	Low		-3.0		V	500 pF	1
H1 High Level	H1H	High		7.0		V		1
H2 Low Level	H2L	Low		-3.0		V	300 pF	1
H2 High Level	H2H	High		7.0		V		1
RG Low Level	V_{RGL}	Low		6.0		V	13 pF	1
RG High Level	V_{RGH}	High		11.0		V		1

Notes:

1. All pins draw less than 10 µA DC current. Capacitance values relative to SUB (substrate).

Timing Requirements

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H		4	10	MHz	1
H1, H2 Rise, Fall Times	t_{H1r} , t_{H1f}	5			%	3
V1, V2 Rise, Fall Times	t_{V1r} , t_{V1f}	5			%	3
V1 - V2 Cross-over	V_{VCR}	-1	0	1	V	
H1 - H2 Cross-over	V_{HCR}			0	V	
H1, H2 Setup Time	t_{HS}	5	10		µs	
RG Clock Pulse Width	t_{RGw}	5			ns	4
V1, V2 Clock Pulse Width	t_{Vw}	20	20		µs	

Timing Characteristics

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Pixel Period (1 Count)	t_e		250		ns	2
Integration Time	t_{int}		-			5
Line Time	t_{line}		1.08		ms	6
Readout Time	$t_{readout}$		4,450		ms	7

Notes:

1. 50% duty cycle values.
2. CTE will degrade above the maximum frequency.
3. Relative to the pulse width (based on 50% of high/low levels).
4. RG should be clocked continuously.
5. Integration time is user specified.
6. $(4145 * t_e) + t_{HS} + (2 * t_{Vw}) = 1.08$ msec
7. $t_{readout} = t_{line} * 4128$ lines.

8.

Frame Timing

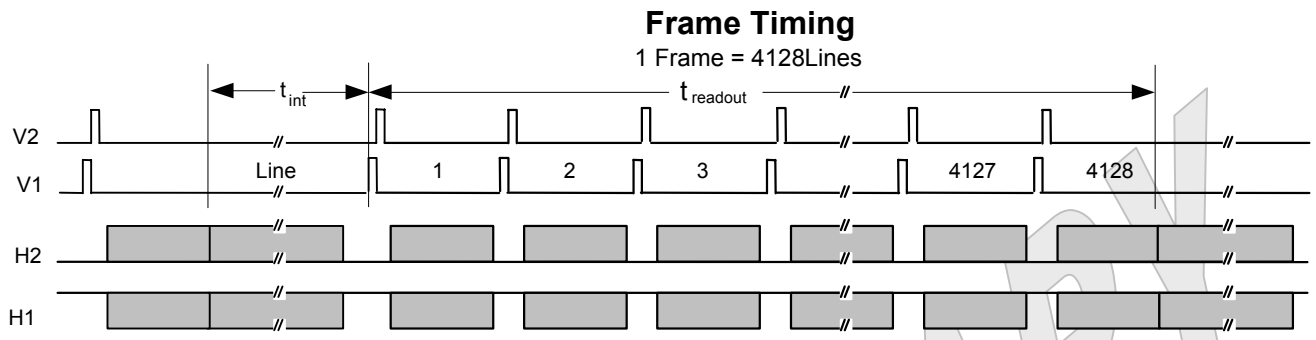


Figure 4 - Frame Timing

Frame Timing Detail

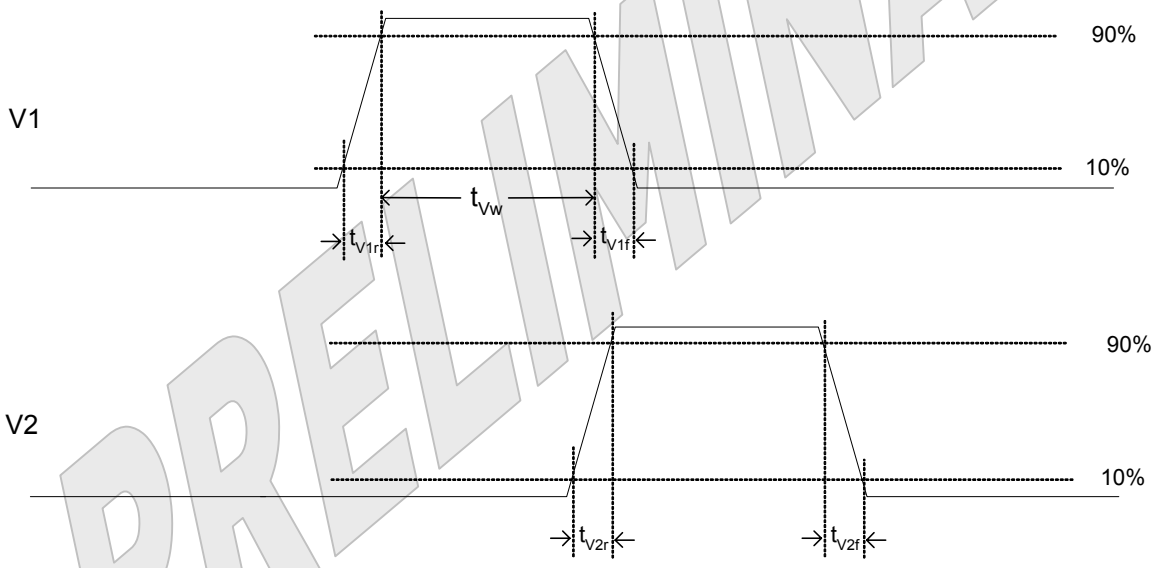


Figure 5 - Frame Timing Detail

Line Timing

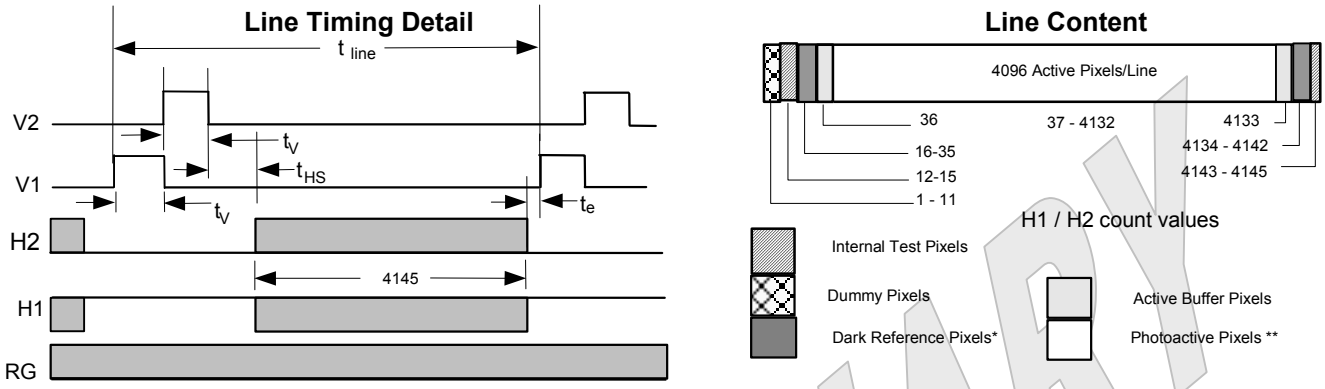


Figure 6 - Line Timing

Pixel Timing Detail

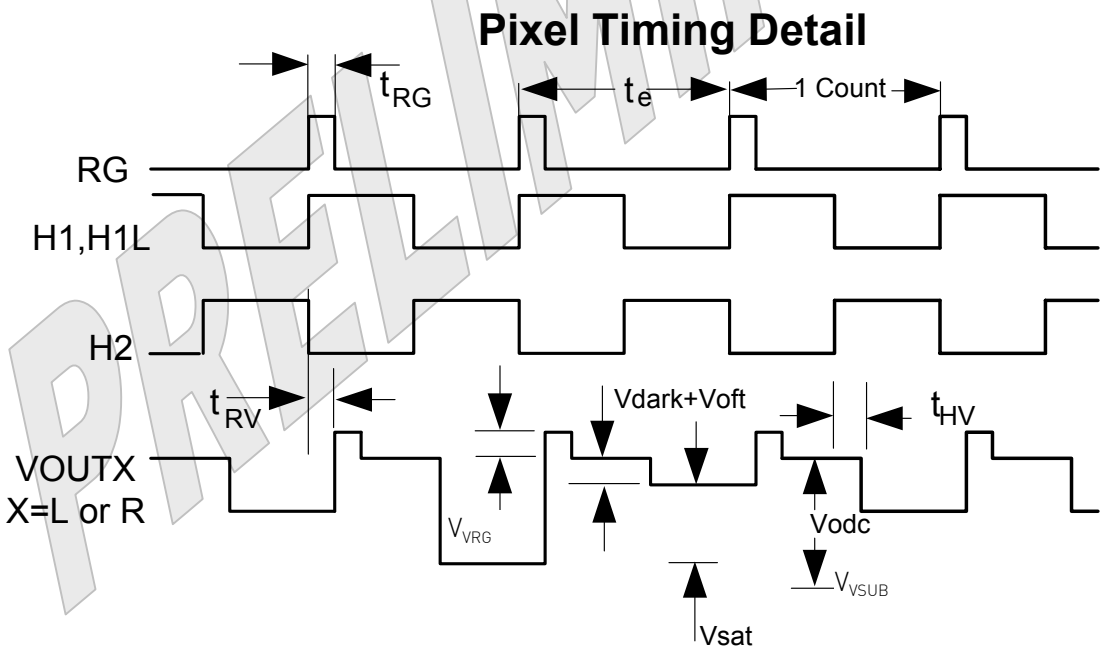


Figure 7 – Pixel Timing

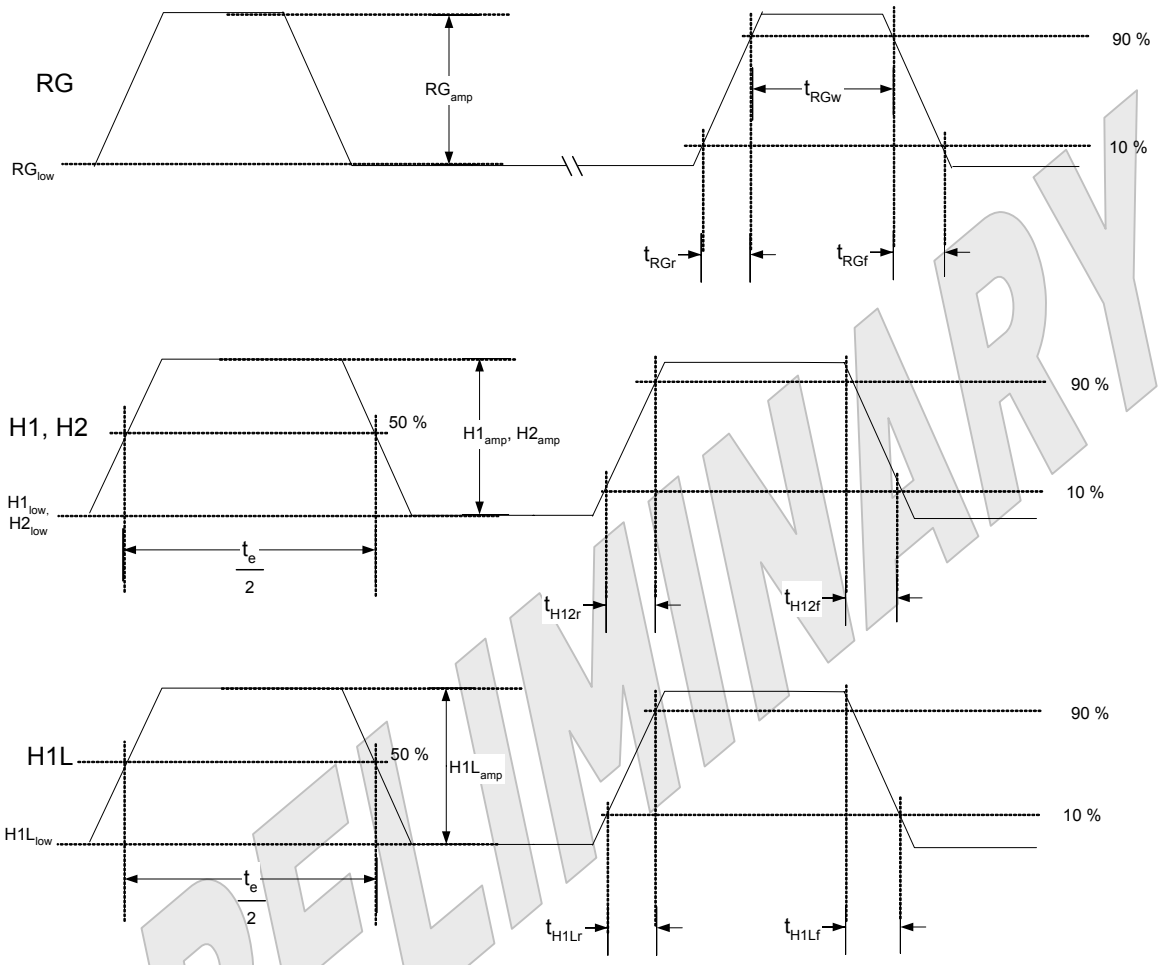


Figure 8 - Pixel Timing Detail

Timing Edge Alignment

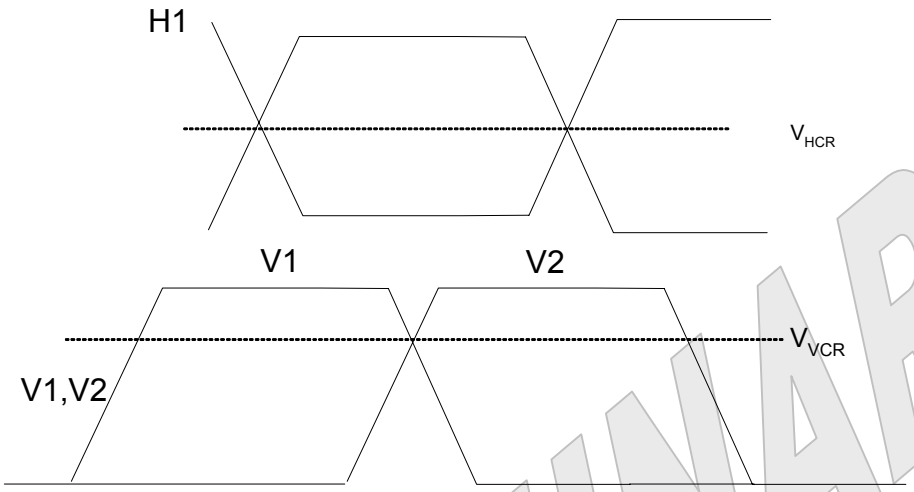
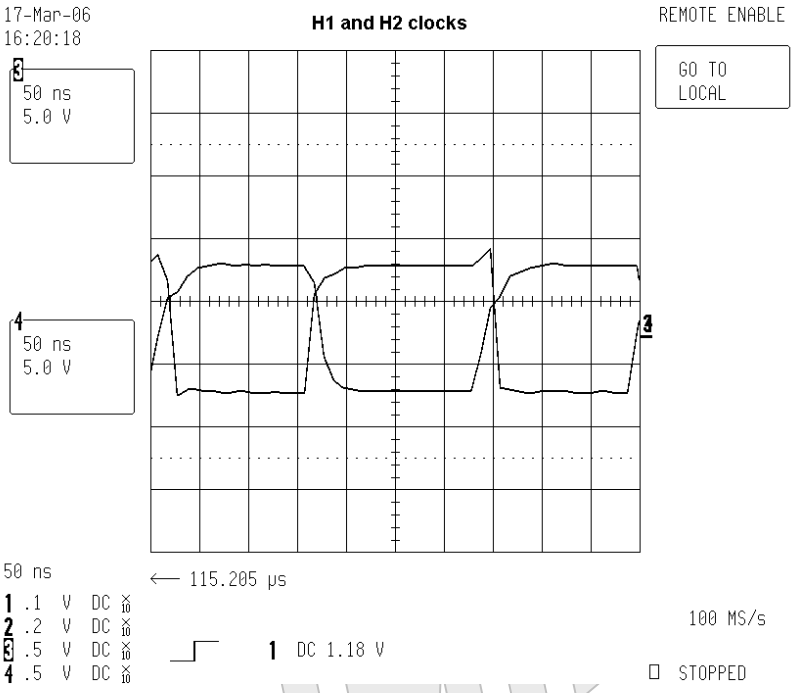


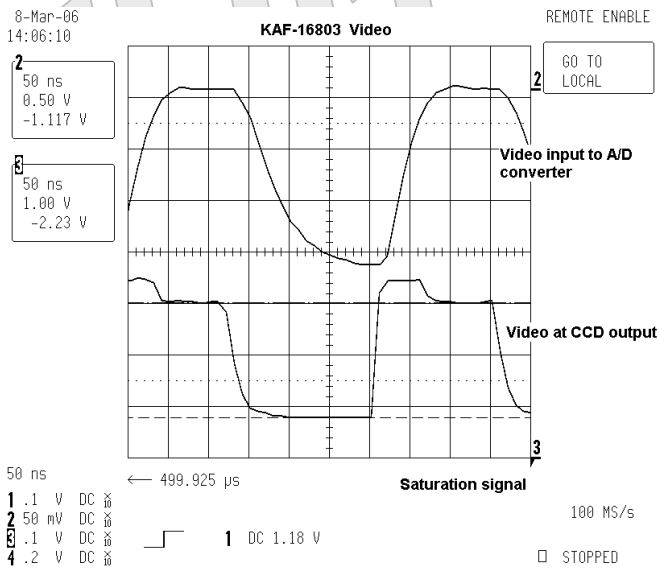
Figure 9 - Timing Edge Alignment

EXAMPLE WAVEFORMS

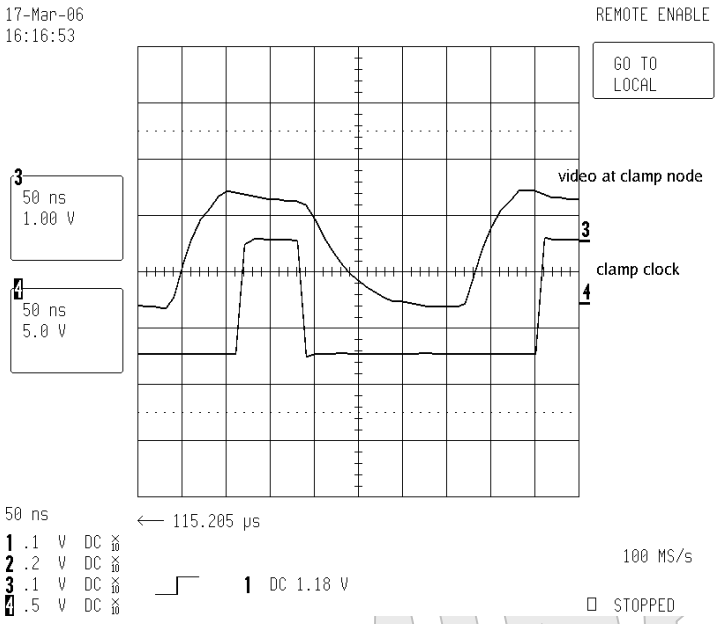
Horizontal CCD clocks



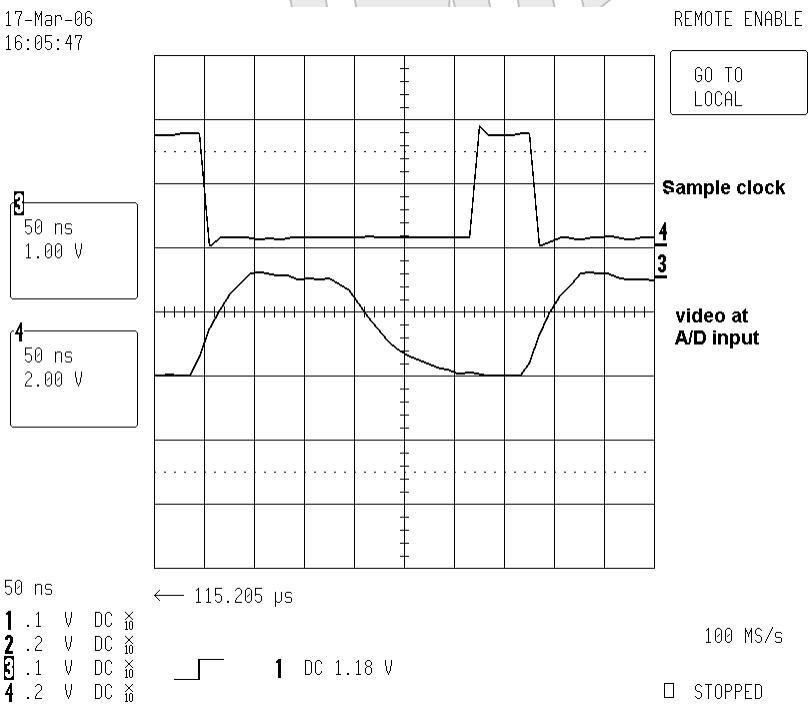
Video Waveform – at the CCD output and bandwidth limited at the analog to digital converter.



Video waveform and clamp clock



Video waveform and sample clock



STORAGE AND HANDLING

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	70	°C	1

Note:

1. Long-term storage toward the maximum temperature will accelerate color filter degradation

ESD

This device contains limited protection against Electrostatic Discharge (ESD) and is rated as a Class 0 device, JESD22 Human Body, and Class A, JESD22 Machine Mode

Devices should be handled in accordance with strict handling precautions. See ISS Application Note MTD/PS-0224, "Electrostatic Discharge Control".

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.

Caution: Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-0237, "Cover Glass Cleaning Procedure for Image Sensors"

SOLDERING RECOMMENDATIONS

Partial Heating Method: 280 °C maximum pin temperature; 10 seconds maximum duration per pin.

MECHANICAL DRAWINGS

PACKAGE